Manual eResources Web Of Science

Universiti Teknologi MARA
Perpustakaan Tun Abdul Razak

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"LIBRARY for ALL"

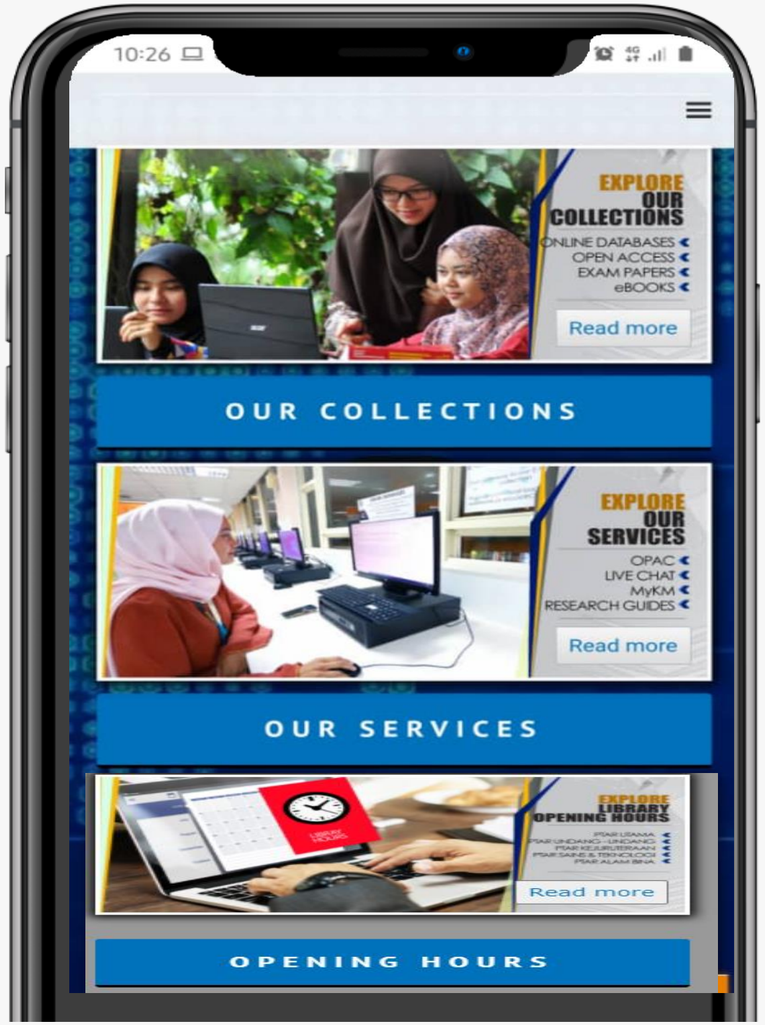
USER MANUAL

Guide 1

1. Go to https://library.uitm.edu.my/

2. From the library portal website there are three categories namely Our Collections, Our Services and Opening Hours.

3. Click 'Our collections' to access eResources Online Database



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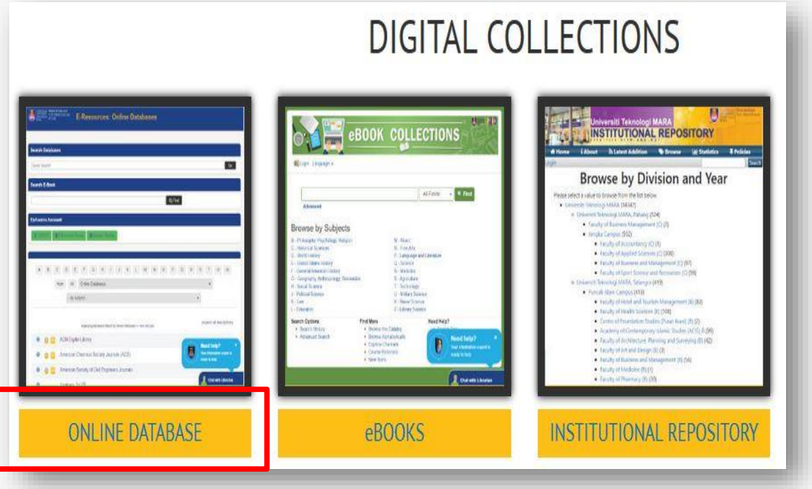
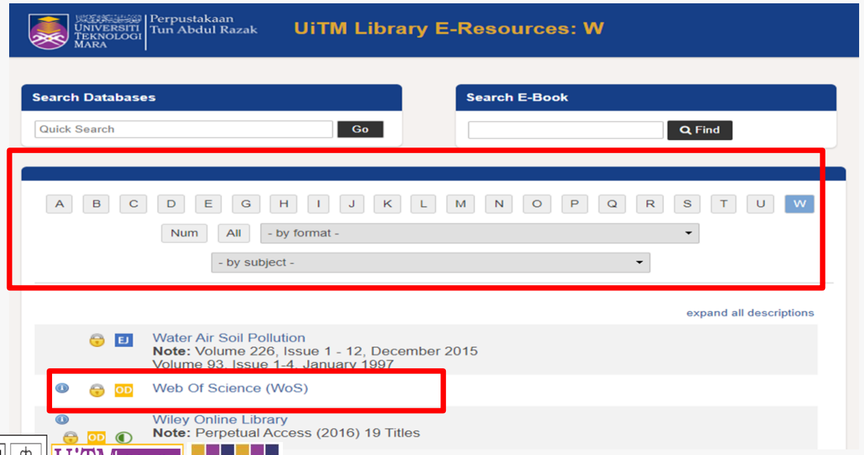
Guide 2



1. In the Digital Collections view, Click Online Database to access the Online Database.



2. User can access Web of Science (WoS) either by alphabet or by format or by subject.

3. Click Web of Science

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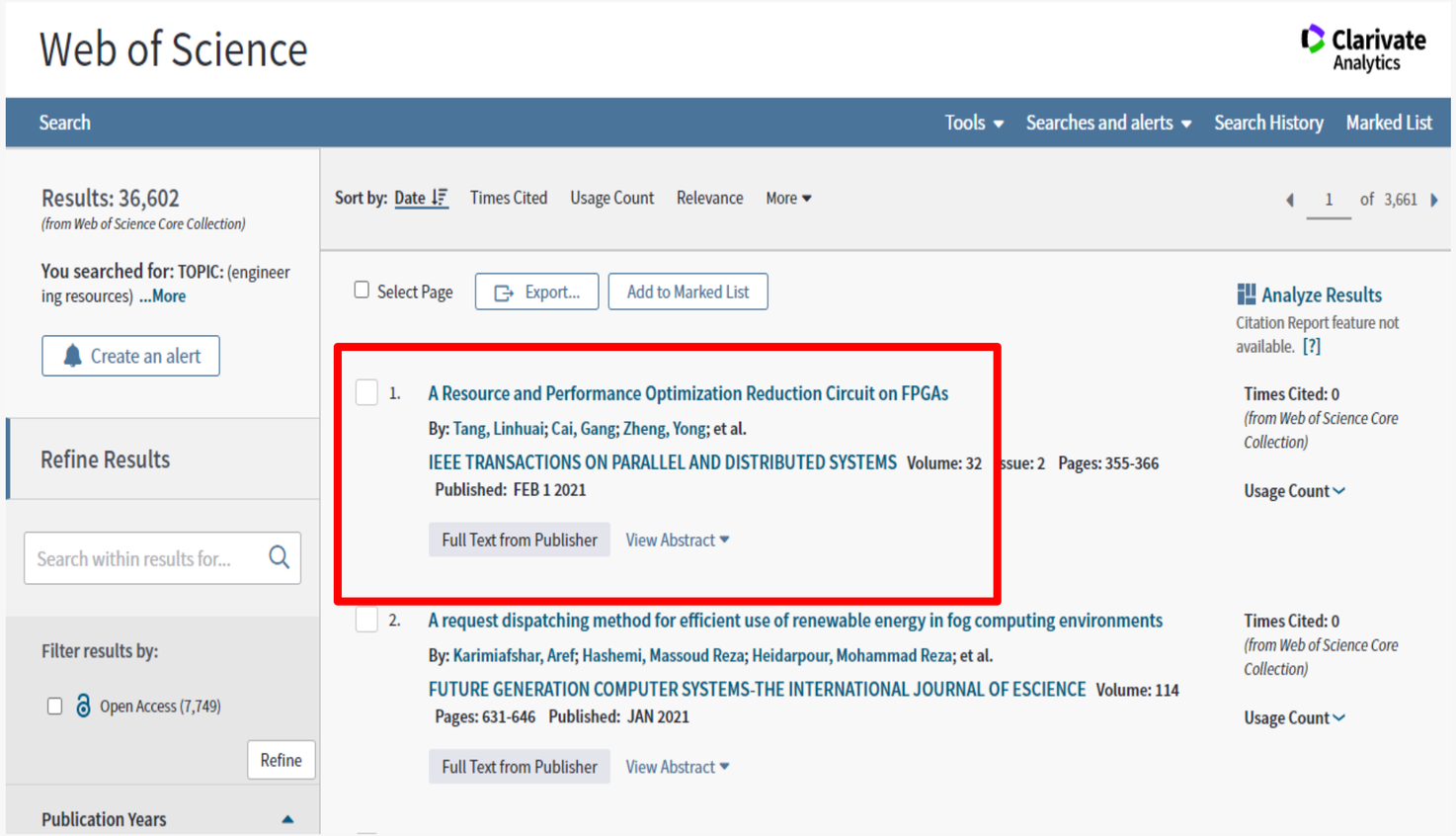
Guide 3



- Click on the title
- User can Download Full text or view Abstract
- Click on Full Text from Publisher to get the pdf full text.
- Note: The pdf full text is available if it is subscribed by the library

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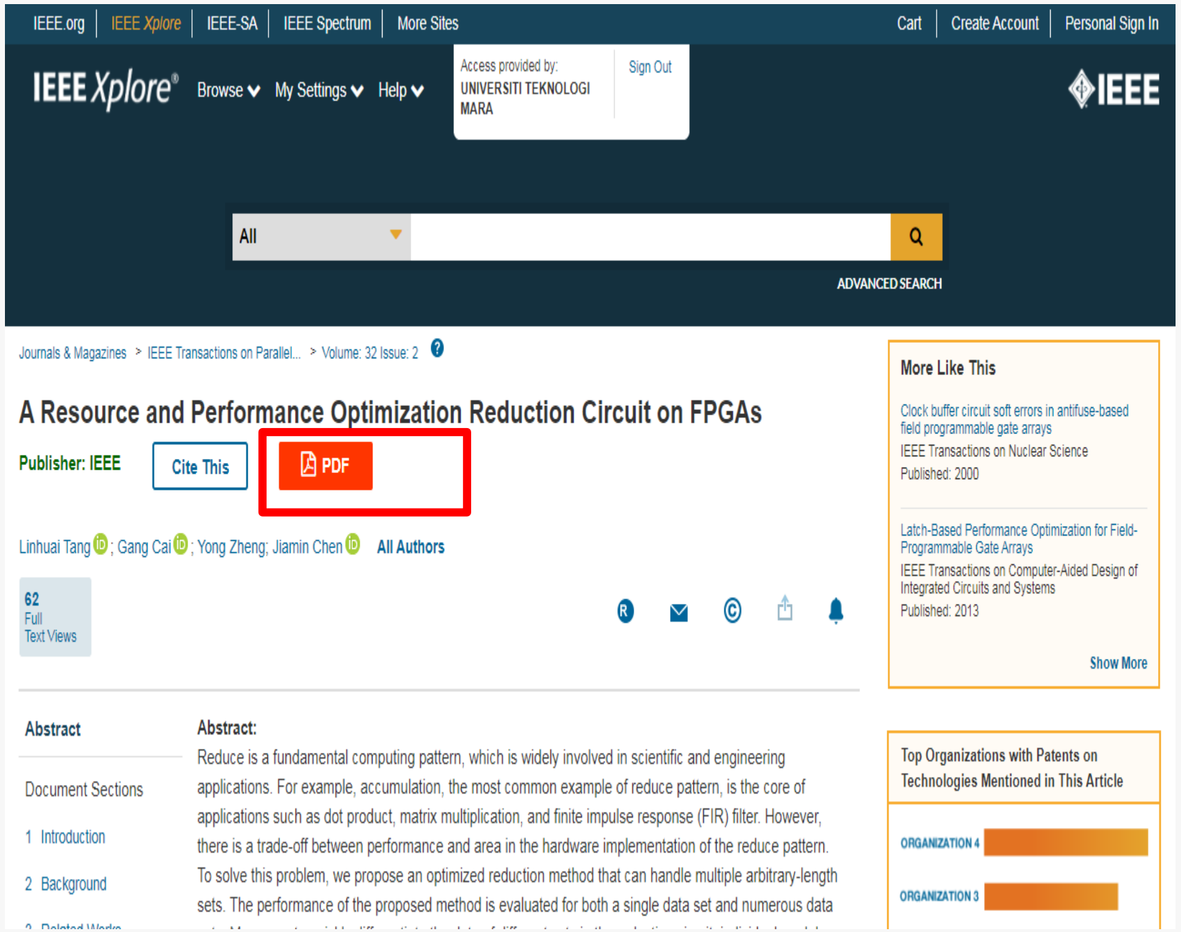
Guide 4



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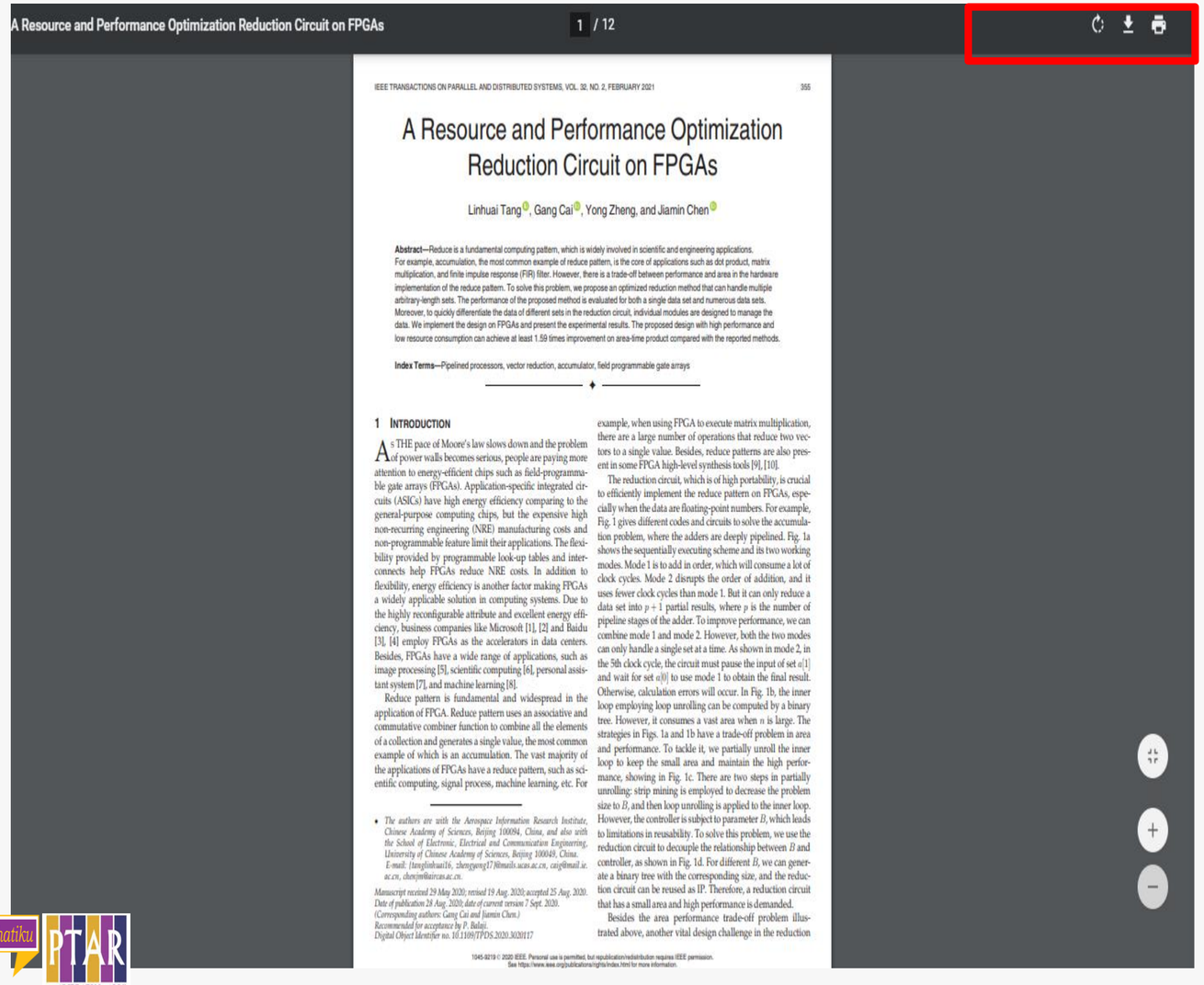
Guide 5



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A Resource and Performance Optimization Reduction Circuit on FPGAs

Linhuai Tang, Gang Cai, Yong Zheng, and Jiamin Chen

Abstract—Reduce is a fundamental computing pattern, which is widely involved in scientific and engineering applications. For example, accumulation, the most common example of reduce pattern, is the core of applications such as dot product, matrix multiplication, and finite impulse response (FIR) filter. However, there is a trade-off between performance and area in the hardware implementation of the reduce pattern. To solve this problem, we propose an optimized reduction method that can handle multiple arbitrary-length sets. The performance of the proposed method is evaluated for both a single data set and numerous data sets. Moreover, to quickly differentiate the data of different sets in the reduction circuit, individual modules are designed to manage the data. We implement the design on FPGAs and present the experimental results. The proposed design with high performance and low resource consumption can achieve at least 1.59 times improvement on area-time product compared with the reported methods.

Index Terms—Pipelined processors, vector reduction, accumulator, field programmable gate arrays

1 Introduction

As THE pace of Moore's law slows down and the problem of power walls becomes serious, people are paying more attention to energy-efficient chips such as field-programmable gate arrays (FPGAs). Application-specific integrated circuits (ASICs) have high energy efficiency comparing to the general-purpose computing chips, but the expensive high non-recurring engineering (NRE) manufacturing costs and non-programmable feature limit their applications. The flexibility provided by programmable look-up tables and interconnects help FPGAs reduce NRE costs. In addition to flexibility, energy efficiency is another factor making FPGAs a widely applicable solution in computing systems. Due to the highly reconfigurable attribute and excellent energy efficiency, business companies like Microsoft [1], [2] and Baidu [3], [4] employ FPGAs as the accelerators in data centers. Besides, FPGAs have a wide range of applications, such as image processing [5], scientific computing [6], personal assistant system [7], and machine learning [8].

Reduce pattern is fundamental and widespread in the application of FPGA. Reduce pattern uses an associative and commutative combiner function to combine all the elements of a collection and generates a single value, the most common example of which is an accumulation. The vast majority of the applications of FPGAs have a reduce pattern, such as scientific computing, signal process, machine learning, etc. For example, when using FPGA to execute matrix multiplication, there are a large number of operations that reduce two vectors to a single value. Besides, reduce patterns are also present in some FPGA high-level synthesis tools [9], [10].

The reduction circuit, which is of high portability, is crucial to efficiently implement the reduce pattern on FPGAs, especially when the data are floating-point numbers. For example, Fig. 1 gives different codes and circuits to solve the accumulation problem, where the adders are deeply pipelined. Fig. 1a shows the sequentially executing scheme and its two working modes. Mode 1 is to add in order, which will consume a lot of clock cycles. Mode 2 disrupts the order of addition, and it uses fewer clock cycles than mode 1. But it can only reduce a data set into $p+1$ partial results, where p is the number of pipeline stages of the adder. To improve performance, we can combine mode 1 and mode 2. However, both the two modes can only handle a single set at a time. As shown in mode 2, in the 5th clock cycle, the circuit must pause the input of set $a[1]$ and wait for set $a[0]$ to use mode 1 to obtain the final result. Otherwise, calculation errors will occur. In Fig. 1b, the inner loop employing loop unrolling can be computed by a binary tree. However, it consumes a vast area when n is large. The strategies in Figs. 1a and 1b have a trade-off problem in area and performance. To tackle it, we partially unroll the inner loop to keep the small area and maintain the high performance, showing in Fig. 1c. There are two steps in partially unrolling: strip mining is employed to decrease the problem size to B, and then loop unrolling is applied to the inner loop. However, the controller is subject to parameter B, which leads to limitations in reusability. To solve this problem, we use the reduction circuit to decouple the relationship between B and controller, as shown in Fig. 1d. For different B, we can generate a binary tree with the corresponding size, and the reduction circuit can be reused as IP. Therefore, a reduction circuit that has a small area and high performance is demanded.

Besides the area performance trade-off problem illustrated above, another vital design challenge in the reduction

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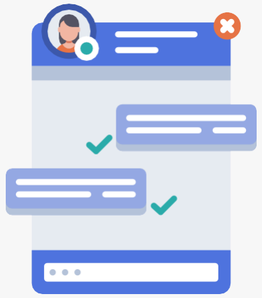

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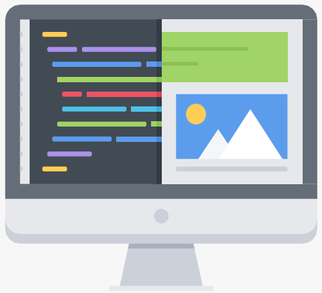

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